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4000-02700

Patent

REMARKS

Claims 1-12 are pending in this application. The Examiner has finally rejected Claims 1-12 on various grounds. The Applicants respectfully traverse these rejections. Reconsideration is requested.

The independent Claims 1, 5, 9 and 11 have been rejected under 35 U.S.C. 102 as being anticipated by the McClear reference, U.S. Patent 5,592,509. The detailed rejection from the first office action was repeated in the final rejection and need not be repeated here again. However, specific errors in the Examiner's reading of McCleary will be discussed.

The Examiner alleges that McClear disclosed an apparatus for preventing bus contention on a data bus when a CPU calls for a read operation followed by a write operation. McClear never uses the term "contention". As stated in McClear at Column 1, lines 51-55, "The invention provides systems such as a transition detecting transceiver coupled between a processor and an array of memory devices, without control lines from the processor to the transceiver."

The Examiner alleges that McClear teaches a transceiver with bus hold circuitry and an output enable input. However, an output enable input is an input for receiving a control line. As quoted above, the transceiver of McClear is "without control lines from the processor to the transceiver." The transceiver of McClear does not have an output enable input.

The Examiner alleges that McClear teaches a transceiver having an input for receiving a CPU chip select signal and an output for providing a peripheral control signal connected to a control input of the peripheral and to the output enable input of the

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transceiver. As quoted above, the transceiver of McClear is "without control lines from the processor to the transceiver." It cannot receive a chip select signal, because it has no control line inputs to receive any control signals. The transceiver of McClear has no control signal outputs connected to a peripheral. Fig. 5 of McClear clearly shows only data bus connections between the transceiver and the peripheral. Even if the transceiver had some form of control signal connection to a peripheral, it could not couple control signals from the processor to the peripheral, since it has no inputs for receiving control signals from a processor.

The Examiner alleges that McClear discloses a buffer in Fig. 5 connected between an address output of a central processing unit and an address input of a peripheral device, the buffer having an output enable input connected to a chip select signal. However, the alleged buffer of Fig. 5 is labeled as a "transceiver" and is the same transceiver shown in Figs. 2 and 3, which has no control signal inputs, not even an output enable input, for receiving any control signals, much less a chip select signal. McClear does not even suggest that the transceiver of Fig. 5 is connected to any address bus inputs or outputs, but instead states that "Circuit 85", i.e. the peripheral, "could be any device which sends and/or receives data..." The transceiver 83 of Fig. 5 is part of a data bus and only has inputs and outputs for receiving and transmitting data.

The Examiner dismissed the Applicants' arguments made in the first response. Errors in the Examiners action are pointed out below.

In the first response, the Applicants pointed out that it is not possible for any part of the McClear transceiver to receive a chip select signal from the CPU, since it has no control signal inputs or outputs whatsoever. In dismissing this argument, the Examiner

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alleges that "the incoming signal from the CPU passes through 171, 173, and 174 of the transceiver. In another word, the control logic 174 does have an input for receiving signal from the CPU." As noted above, the transceiver has no control signal inputs or outputs. The transceiver cannot provide CPU control signals to any of its internal circuits unless it receives the CPU control signals first. Since the transceiver does not receive a CPU chip select or any other control signal, it cannot provide such non-existent signals to itself. The transceiver receives and transmits only data.

The Applicants pointed out that "it is not possible for the control logic to be connected to a control input of the peripheral and to the output enable input of the peripheral." In dismissing this argument, the Examiner alleged that the transceiver of McClear "is connected to the control input of a peripheral downstream of the transceiver. Therefore it is clear that control logic 174 is connected to the control input of the peripheral downstream of the transceiver." However, as pointed out above, the transceiver of McClear has no control signal inputs or outputs. Its only connection to the peripheral is a data bus.

The Examiner further alleges that "The control logic 174 provides an output enable control line for driver 176, for example, which provides an output enable input for the transceiver (the line connecting 176 to A)." However, McClear teaches that the collision arbitration signal to the driver 176 allows the driver 176 to drive data onto the data bus A. The collision arbitration signal itself is completely internal to the transceiver and is never coupled to either part A or B of the data bus.

From the above remarks it is clear that the McClear reference provides no teaching concerning the coupling of control signals to, from or between a CPU and a

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transceiver or between a transceiver and a peripheral device. McClear does not and cannot provide any teaching of a modified control signal which allows the peripheral and the transceiver to go three state before the end of a read cycle to prevent contention when the read cycle is followed by a write cycle.

The Applicants submit that they have shown the pending claims to be patentable over the cited reference. Allowance of Claims 1-12 is requested.

The Commissioner is hereby authorized to charge payment of any further fees associated with any of the foregoing papers submitted herewith, or to credit any overpayment thereof, to Deposit Account No. 21-0765, Sprint.

Applicants respectfully submit that the present application is in condition for allowance. If the Examiner has any questions or comments or otherwise feels it would be helpful in expediting the application, he is encouraged to telephone the undersigned at (972) 731-2288.

Respectfully submitted,
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